GS2988 Dual-Slew-Rate, Cable Driver with 3Gb/s Capability

Features

- SMPTE 424M, SMPTE 292M and SMPTE 259M compliant
- Supports DVB-ASI at 270Mb/s
- Supports data rates from 270Mb/s to 2.97Gb/s
- Wide common-mode range input buffer
  - 100mV sensitivity
  - supports DC-coupling to industry-standard differential logic
  - on-chip 100Ω differential data input termination
- Input signal trace equalization
- Differential coaxial-cable-driving output
  - selectable slew rates
  - adjustable output swing from 500mVpp to 1800mVpp
  - DISABLE control
- Robust output signal presence function
- Excellent output eye quality
- Power supply operation at 3.3V or 2.5V
- 110mW power consumption (2.5V supply)
- Operating temperature range: -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
  - Drop-in compatible to the GS2978
- Pb-free and RoHS compliant

Applications

- SMPTE 424M, SMPTE 292M and SMPTE 259M coaxial cable serial digital interfaces

Description

The GS2988 is a high-speed BiCMOS integrated circuit designed to drive one to two 75Ω coaxial cables.

The GS2988 may drive data rates up to 2.97Gb/s and provides two selectable slew rates in order to achieve compliance to SMPTE 424M, SMPTE 292M and SMPTE 259M.

The GS2988 accepts industry-standard differential input levels including LVPECL and CML.

Input trace equalization compensates for up to 10 inches of FR4 trace loss while in HD and 3G modes. This feature can be disabled using the $\overline{\text{EQ\_EN}}$ pin.

The $\overline{\text{DISABLE}}$ pin powers-down the entire device.

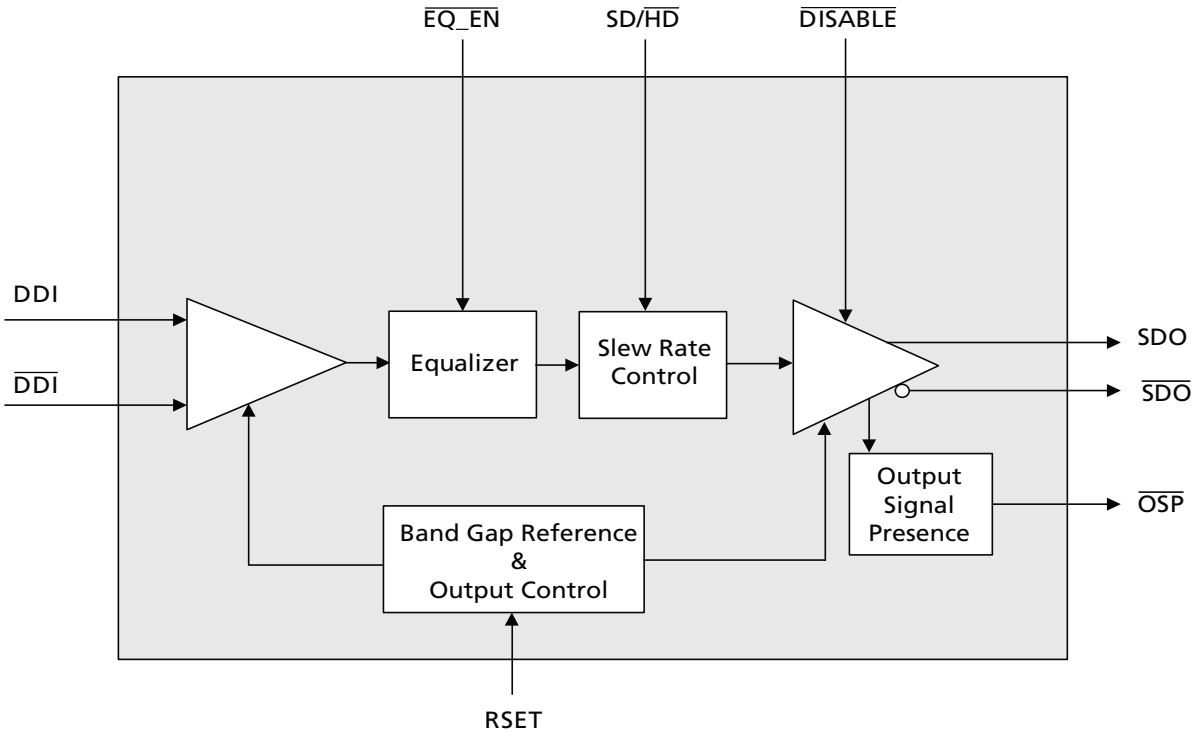
The GS2988 features adjustable output swing using an external bias resistor. The single-ended output swing is adjustable from 500mVpp to 1800mVpp.

An output signal presence function, the $\overline{\text{OSP}}$ pin, indicates whether an active signal is present at the output of the GS2988.

The GS2988 can be powered from either a 3.3V or a 2.5V supply. Power consumption is typically 110mW using a 2.5V power supply.

The GS2988 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
4	155552	–	December 2010	Corrected the Marking Diagram.
3	155359	–	November 2010	Clarified the functionality of the EQ_EN pin in Table 1-1: Pin Descriptions and throughout the document.
2	155070	–	October 2010	Updated Typical Application Circuit.
1	153602	–	February 2010	Converted document to Data Sheet.
0	153455	–	January 2010	Converted document to Preliminary Data Sheet. Changed Additive jitter numbers in Table 2-2: AC Electrical Characteristics.
B	152690	–	October 2009	Updates to Section 2. Electrical Characteristics. Corrections to Section 3. Input/Output Circuits.
A	151623	–	April 2009	New document.

Contents

1. Pin Out

1.1 Pin Assignment

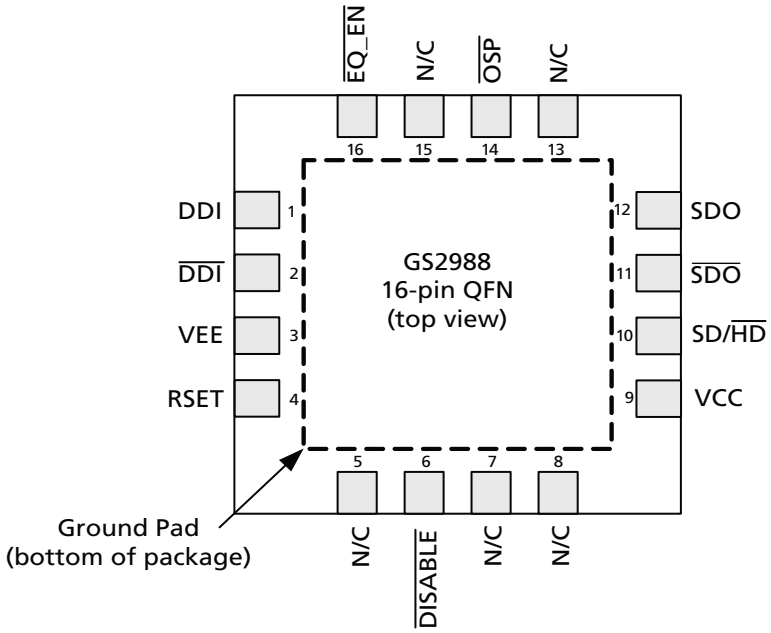


Figure 1-1: 16-Pin QFN

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1, 2	DDI, $\overline{\text{DDI}}$	Input	Serial data differential input.
3	VEE	Power	Most negative power supply connection for the input buffer and core. Connect to GND.
4	RSET	Input	External output amplitude control resistor connection.
5, 7, 8, 13, 15	N/C	–	No Connect. These pins are not connected internally.
6	$\overline{\text{DISABLE}}$	Input	Control signal input. When set LOW, the entire device is powered-down. When set HIGH, the SDO/$\overline{\text{SDO}}$ pins will output a serial data signal. **NOTE:** if this pin is left floating, the serial data output will be **enabled**.
9	VCC	Power	Most positive power supply connection. Connect to 3.3V or 2.5V.

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
10	SD/$\overline{HD}$	Input	Control signal input. When set HIGH, the serial data output will meet the SMPTE 259M rise/fall time specification. When set LOW, the serial output will meet the SMPTE 292M and SMPTE 424M rise/fall time specification. **NOTE:** if this pin is left floating, the serial data output will meet the SMPTE 259M rise/fall time specification.
11, 12	$\overline{SDO}$/ SDO	Output	Serial data differential output.
14	$\overline{OSP}$	Output	Output signal presence status signal output. Signal levels are LVCMOS/LVTTL compatible. Indicates presence of a valid output signal. When the $\overline{OSP}$ pin is LOW, a good input signal has been detected within the output stage pre-driver. When this pin is HIGH, the output signal is invalid at the output of the pre-driver.
16	$\overline{EQ\_EN}$	Input	Control signal input. When set LOW, trace-equalization is turned ON. When set HIGH, trace-equalization is turned OFF. **NOTE 1:** if this pin is left floating, trace-equalization is turned OFF. **NOTE 2:** this pin must be pulled HIGH or left floating for operation in SD mode.
–	Center Pad	Power	Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 15.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	2.5kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	3.3V Typical	3.135	3.3	3.465	V	–
		2.5V Typical	2.375	2.5	2.625	V	–
Power Consumption (2.5V)	P_D	SDO/$\overline{SDO}$ enabled	–	110	130	mW	1
		SDO/$\overline{SDO}$ disabled	–	3	5	mW	1
Power Consumption (3.3V)		SDO/$\overline{SDO}$ enabled	–	155	183	mW	1
		SDO/$\overline{SDO}$ disabled	–	4	6	mW	1
Supply Current	I_S	VCC = 3.3V	–	47	53	mA	1
		VCC = 2.5V	–	44	50	mA	1
		Power-down	–	1	1.8	mA	1
Output Voltage	V_{CMOUT}	Common mode	–	V_{TERM} - V_{OUT}	–	V	–
Input Voltage	V_{CMIN}	Common mode	1.4 + $\Delta V_{DDI}/2$	–	V_{CC} - $\Delta V_{DDI}/2$	V	–
SD/$\overline{HD}$, $\overline{DISABLE}$, $\overline{EQ\_EN}$ Input	V_{IH}	I_{IH} <= 150µA	1.7	–	–	V	–
	V_{IL}	I_{IL} <= 150µA	–	–	0.8	V	–
OSP Drive Strength	–	–	2	–	–	mA	–

NOTES:

1. Power consumed in GS2988 only. Termination resistors draw extra current.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	.27	–	2.97	Gb/s	1
Additive jitter	–	2.97Gb/s	–	10	–	ps_{p-p}	2
	–	1.485Gb/s	–	10	–	ps_{p-p}	2
	–	270Mb/s	–	30	–	ps_{p-p}	2
Rise/Fall time	t_r, t_f	SD/$\overline{HD}$=0	–	–	135	ps	3
	t_r, t_f	SD/$\overline{HD}$=1	400	–	800	ps	3
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	HD/3G modes only	–	–	35	ps	–
Duty cycle distortion	–	SD/$\overline{HD}$=0, 2.97Gb/s	–	–	14	ps	4, 5
	–	SD/$\overline{HD}$=0, 1.485Gb/s	–	–	20	ps	4, 5
	–	SD/$\overline{HD}$=1	–	–	50	ps	4, 5
Overshoot	–	SD/$\overline{HD}$=0,	–	–	10	%	4
Output Return Loss	ORL	5 MHz – 1.485GHz	17	19	–	dB	6
		1.485GHz – 2.97GHz	13	15	–	dB	6
Output Voltage Swing	V_{OUT}	R_{SET} = 750Ω	750	800	850	mV_{p-p}	4
Input Voltage Swing	$\triangle V_{DDI}$	Guaranteed functional.	100	–	250	mV_{p-pd}	–
		Guaranteed to meet all published specifications.	250		2200	mV_{p-pd}	–
Output Enable Delay	–	–	–	–	100	ns	–
Output Disable Delay	–	–	–	–	80	ns	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Turning on input trace equalization will reduce jitter in most applications.
3. Rise/Fall time measured between 20% and 80%.
4. Single-ended into 75Ω external load.
5. Calculated as the actual positive bit-width compared to the expected positive bit-width using a 1010 pattern.
6. ORL depends on board design. The GS2988 achieves this specification on Gennum's evaluation boards.

3. Input/Output Circuits

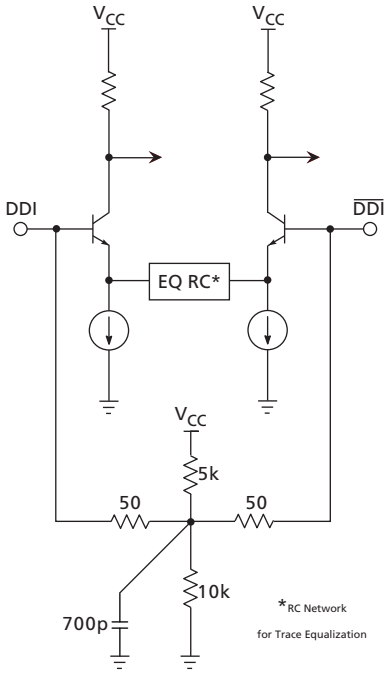


Figure 3-1: Differential Input Stage (DDI/DDI)

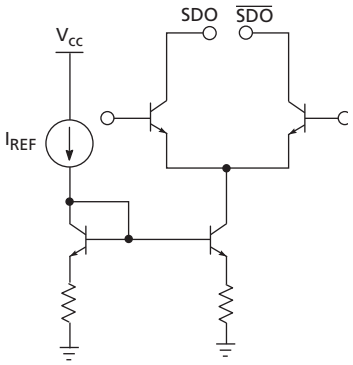


Figure 3-2: Differential Output Stage (SDO/SDO)

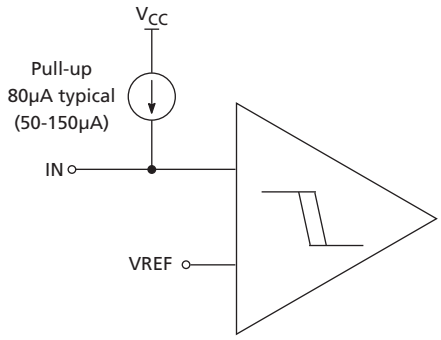


Figure 3-3: Control Input (DISABLE, SD/HD, EQ_EN)

4. Detailed Description

4.1 Serial Data Input

The GS2988 features a differential input buffer with on-chip 100Ω differential termination.

The serial data input signal is connected to the DDI and $\overline{\text{DDI}}$ input pins of the device.

Input signals can be single-ended or differential, DC or AC-coupled.

The serial data input buffer is capable of operation with any binary coded signal that meets the input signal level requirements, in the range of 270Mb/s to at least 2.97Gb/s.

The input circuit is self-biasing to allow for simple AC or DC-coupling of input signals to the device.

4.2 Input Trace-equalization

The GS2988 features fixed trace-equalization to compensate for PCB trace dielectric losses.

NOTE: This feature is not available in SD mode, and therefore trace-equalization must be disabled when operating in this mode.

The trace-equalization has two settings, OFF and ON. ON invokes a typical 3dB gain value at 1.5GHz. This value is optimized for compensating the high-frequency losses associated with approximately 10 inches of 5-mil stripline in FR4 material.

Table 4-1: Input Trace-Equalization

$\overline{\text{EQ\_EN}}$	Function
0	Typical 3dB Trace Equalization
1	Trace Equalization OFF
Floating	Trace Equalization OFF

4.3 Serial Data Output

The GS2988 features a current-mode differential output driver capable of driving up to 1800mVpp single-ended into a 1m length of 75Ω cable terminated at both ends.

The output signal amplitude or swing is user configurable using an external RSET resistor.

The SDO/$\overline{\text{SDO}}$ pin of the device provide the serial data outputs.

4.3.1 Slew Rate Selection (Rise/Fall Time Requirement)

The GS2988 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the SD/$\overline{\text{HD}}$ input pin.

Table 4-2: Slew Rate Selection

SD/$\overline{HD}$	Rise/Fall Time
0	SMPTE 424M & 292M compliant
1	SMPTE 259M compliant
Floating	SMPTE 259M compliant

4.4 Output Disable

The GS2988 supports an output disable function for the serial data differential output.

Control of this function is determined by the setting of the $\overline{DISABLE}$ control pin.

The serial output disable ($\overline{DISABLE}$), disables power to the entire device. When asserted LOW, the SDO/$\overline{SDO}$ output driver is powered-down.

Table 4-3: Output Disable

$\overline{DISABLE}$	SDO/$\overline{SDO}$
0	All Chip Power Down
1	Operational
Floating	Operational

4.5 Output Signal Presence Indicator ($\overline{OSP}$)

The GS2988 supports an output signal presence indicator function.

The output signal presence pin ($\overline{OSP}$) is an active-low output that indicates when a valid output signal has been detected at the pre-driver output.

The output signal presence function measures signal-edge energy to indicate that the pre-driver to the serial data outputs is toggling.

Table 4-4: Output Signal Presence Indicator

Pre-Driver Output	$\overline{OSP}$ Pin
Valid signal present	0
No valid signal present	1

4.6 Output Amplitude (RSET)

The output amplitude of the GS2988 can be adjusted by changing the value of the RSET resistor as shown in Figure 4-1. For an 800mV$_{p-p}$ output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The RSET resistor is part of an internal DC feedback loop in the GS2988. The resistor should be placed as close as possible to the R_{SET} pin, and connected directly to the VCC plane (traces/wires may cause instability). In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the RSET resistor and the RSET pin.

NOTE: Care should be taken when considering layout of the RSET resistor. Please refer to Section 5.1 for more details.

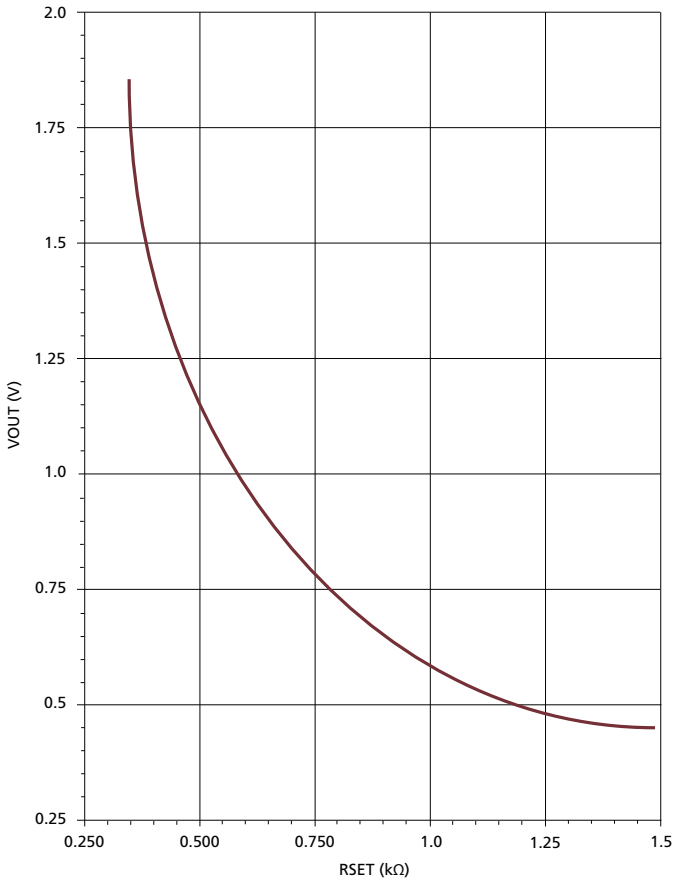


Figure 4-1: V_{OUT} vs. RSET

In order to determine the best starting value for Rset, the following formula should be used:

Rset = 8*(Rtrm/VoutppSE)

Where ***VoutppSE*** is in Volts, and both resistances are in Ω.

Rtrm is the value of the termination resistors, which should be equal to the characteristic impedance of the cable, and is typically 75Ω.

The cable must be short (≤1m), and terminated at both ends for the formula to be valid.

Example: For a 75Ω cable, Rtrm = 75Ω (at both ends), VoutppSE = 800mV

Rset = 8*(75/0.8) = 750Ω

This formula is not valid for long, unterminated, or improperly terminated cables.

This formula should be considered as a starting point, and actual swing values may vary based on layout. Also, for large output swings (>1040mV), smaller Rset values may be required in order to achieve the desired output swing level at HD and 3G data rates.

Table 4-5: Typical RSET Values

Output Swing (mV)	RSET (Ω)
1800*	332
800	750
500	1210

*NOTE: In order to generate output swings greater than 1040mV, VCC_TERM must be connected to a 5V supply.

4.7 Output Return Loss Measurement

The GS2988 has a feature which allows users to measure ORL reliably while the device is still powered. The device can be put into a BALANCE mode which prevents the outputs from toggling while the device is powered on, allowing the ORL to be measured while the device is still powered.

When $\overline{\text{EQ\_EN}}$ is LOW while SD/$\overline{\text{HD}}$ is HIGH, the device goes into BALANCE mode. This mode is used during ORL measurement, disabling the AC signal path of the device without powering it down. When in BALANCE mode, the device produces equal pull-down currents in both differential shoulders of the serial data differential output, effectively stopping the output at the output common mode voltage level. Gennum recommends using BALANCE mode when measuring ORL with 2.5V termination voltage.

5. Application Information

5.1 PCB Layout

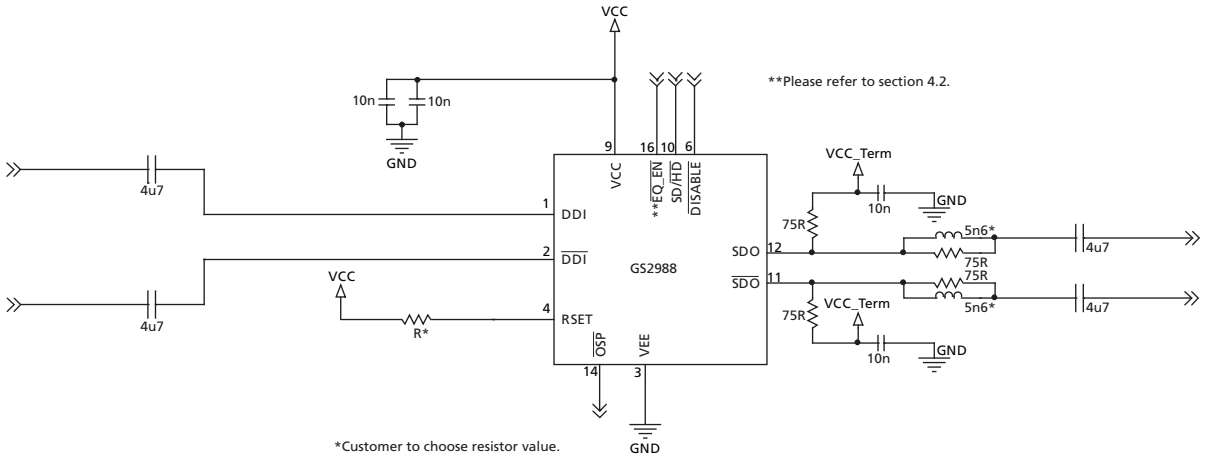
Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance
- The PCB ground plane is removed under the GS2988 output components to minimize parasitic capacitance (NOTE: care should be taken, as removing too much of the plane will make the system susceptible to EMI)
- The PCB ground plane is removed under the GS2988 RSET pin and resistor to minimize parasitic capacitance. The RSET resistor should be directly connected to the VCC plane
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high-speed traces
- High-speed traces are curved to minimize impedance variations due to change of PCB trace width

NOTE: For more recommendations on Trace Lengths, ORL Inductor Values and other PCB Layout Considerations, please refer to Gennum's GS2989 Design Guide (Doc ID 52070).

5.2 Typical Application Circuit



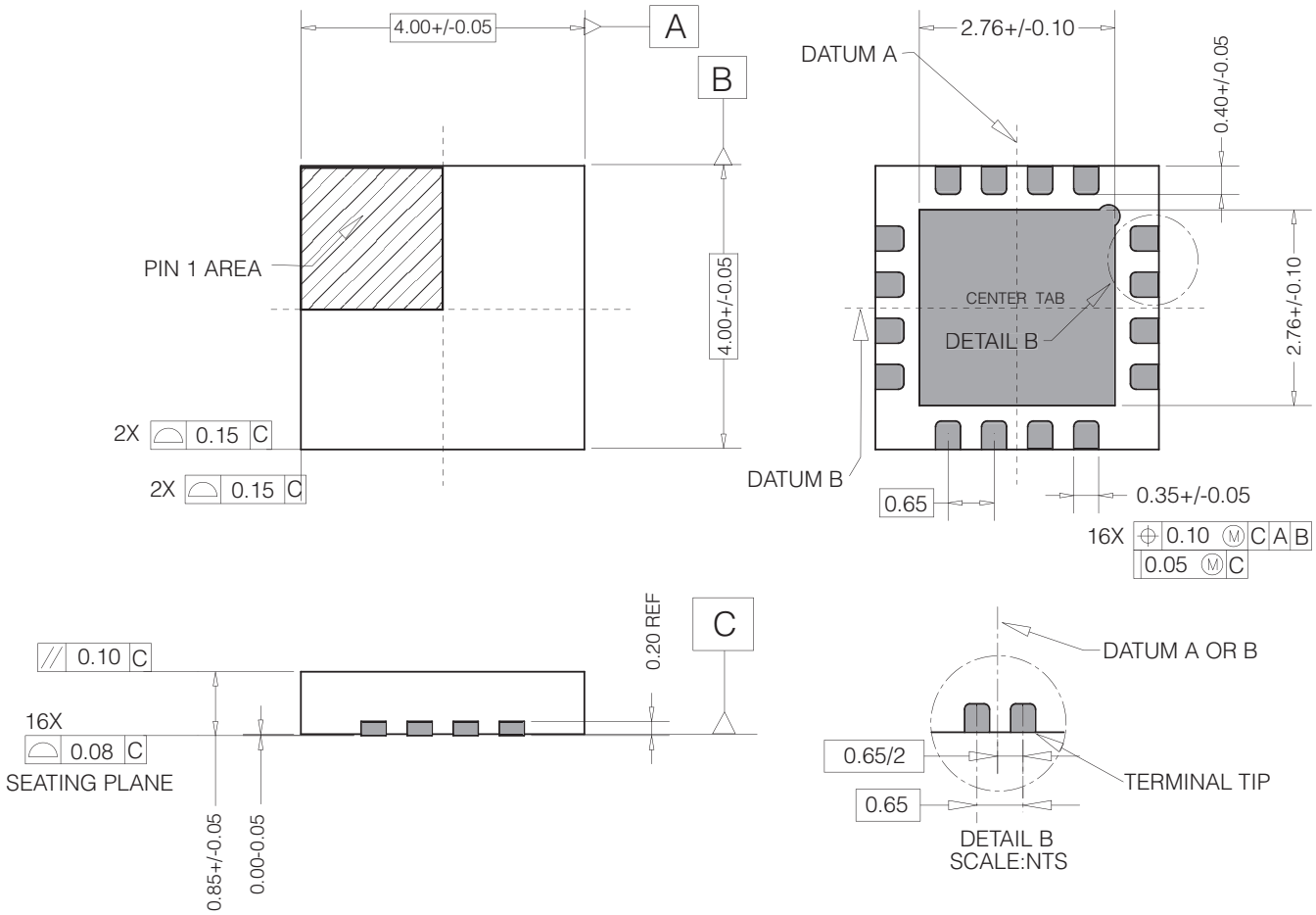
NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise stated.

* Typical value: varies with layout, and represents a trade-off between good eye shape and output return loss.
5n6 is the optimum value for an 800mV output swing.
6n8 is the optimum value for an 1800mV output swing.

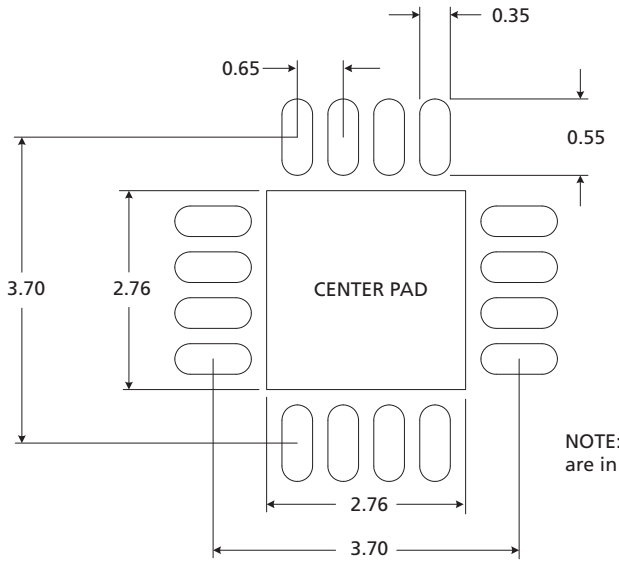
Figure 5-1: Typical Application Circuit

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package type / dimensions / pad pitch	16-pin QFN / 4mm x 4mm / 0.65mm
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, Ψ	11.0°C/W
Pb-free and RoHS compliant, Halogen-free	Yes

6.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 6-1.

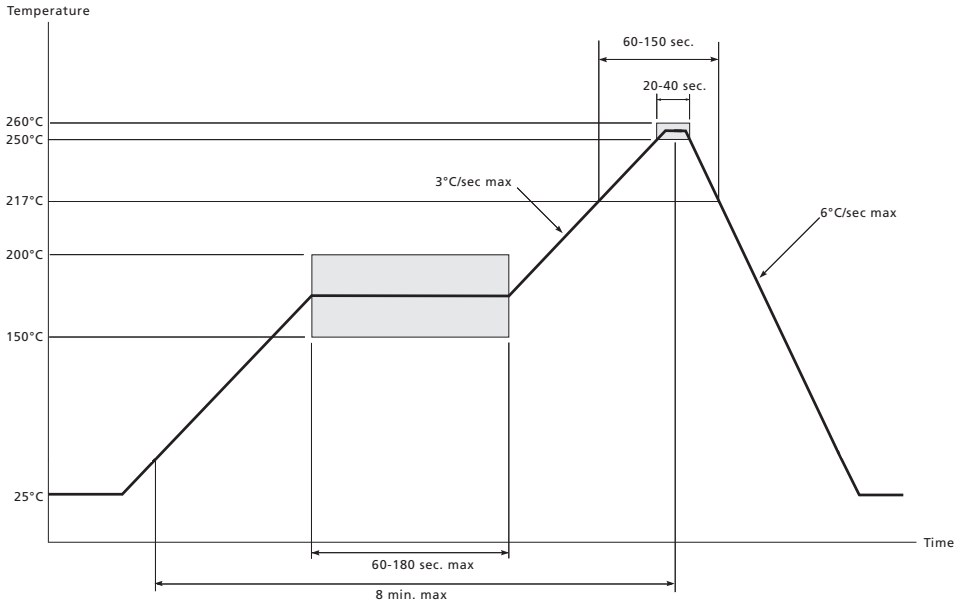
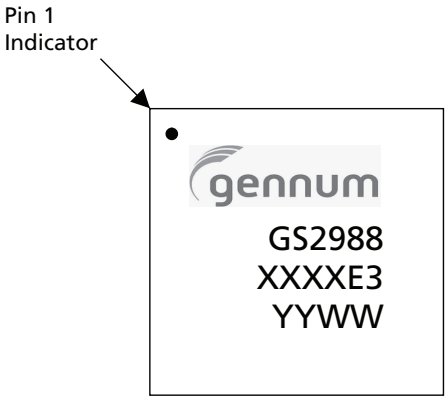


Figure 6-1: Maximum Pb-free Solder Reflow Profile (Preferred)

6.5 Marking Diagram



Instructions:	
GS2988	Package Mark
XXXX	Last 4 digits (excluding decimal) of SAP Batch Assembly (FIN) as listed on Packing Slip
E3	Pb-free & Green indicator
YYWW	Date Code

6.6 Ordering Information

	Part Number	Package	Temperature Range
GS2988	GS2988-INE3	16-pin QFN	-40°C to 85°C
GS2988	GS2988-INTE3	16-pin QFN 250pc Reel	-40°C to 85°C
GS2988	GS2988-INTE3Z	16-pin QFN 2,500pc Reel	-40°C to 85°C

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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